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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/642,214 | 08/18/2003 | Fumitoshi Yamamoto | 67161-081 | 2238 |

7590 09/22/2006

McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

| EXAMINER |
|---|
| LEJA, RONALD W |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/642,214 | YAMAMOTO ET AL. | |
| | Examiner | Art Unit | |
| | Ronald W. Leja | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 2001/0007521 A1).

Chen discloses and ESD surge protection circuit having an input terminal (40) and a first transistor (pnp) and a second transistor (npn) (see Figure 11B). A field oxide film (60) is formed on the surface of the substrate and the pn junction of said emitter and said base of said first transistor (pnp) is considered to be in contact (via the surface of the substrate) with one end of the field oxide film (60) and a pn junction of said collector and said base is considered to be in contact (via the surface of the substrate) with another end of said field oxide film (60).

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Tong et al. (6,867,957).

Tong et al. disclose a semiconductor device comprising ESD surge protection electrically connected to a input terminal (Pad) wherein a first transistor (14) is more susceptible to breakdown than the second transistor (22) (see Column 2, lines 28-51). The base width of the first transistor is smaller than the that of the second transistor.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong et al. in view of Young et al. (4,760,433).

These set of claims are drawn to lowering the susceptibility of the first transistor to breakdown over that of the second transistor by configuring a region attaining the function of a base with having a higher impurity density. Tong et al. disclose adjusting the base width for lowering such susceptibility, but do not appear to disclose adjustment of impurities for base regions. However, Young et al. teach that it is known to increase the impurity of base regions in ESD surge protection transistors so as to increase the beta and decrease the collector-base breakdown. Therefore, it would have been obvious to increase the impurity of the base region of the first transistor so as to further increase sensitivity to surges (esp. dependent upon chip

application), and thereby, trigger the protection sooner and to do so by saving semiconductor surface real estate. This results in a compact but more protective protection circuit.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over tong et al. in view of Voldman et al. (US 2002/0186068 A1).

Claim 4 is drawn to a specifically arranged protection circuit. Voldman et al. teach ESD surge protective circuits wherein the circuit in Figure 5 reads upon the connections between the first and second transistors found within Claim 4. It would have been obvious to apply the circuit of voldman et al. and have different base widths to the two transistors, for example, to the circuit in Figure 5 of Voldman et al., wherein the first transistor (trigger device) has a smaller base width than the base width of the second transistor (clamp device), thereby increasing the sensitivity of the ESD surge protective circuit to ESD/surge events, resulting in increased protection to any attached load.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong et al. in view of Chen.

Claims 5 and 6 are each drawn to a specifically-connected protective circuits having the two transistors. Chen teaches protective circuits wherein the circuit found in Figure 10B is considered to read upon the claim language found in Claim 5. See also Figure 9, wherein the emitter of the first transistor (pnp) is considered to be electrically connected to said base of the first transistor and said collector of said second transistor (npn) (via P-sub). The connections of the two transistors found in the language of Claim 6 are different from that of Claim 5, but essentially the two different circuits merely offer a voltage divider with the resistance and first transistor

so as to trigger the second transistor. As such, it would have been obvious to apply any circuit, such as the one found in Claim 6 and the circuits of Chen and have different base widths to the two transistors, for example, to the transistors in the circuits of Figures 9 and 10B, wherein the first transistor (npn) has a smaller base width than the base width of the second transistor (pnp), thereby increasing the sensitivity of the ESD surge protective circuit to ESD/surge events, resulting in increased protection to any attached load.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W. Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ronald W Leja
Primary Examiner
Art Unit 2836

rwl
September 16, 2006